Analog Design Using g_m/I_d and f_t Metrics

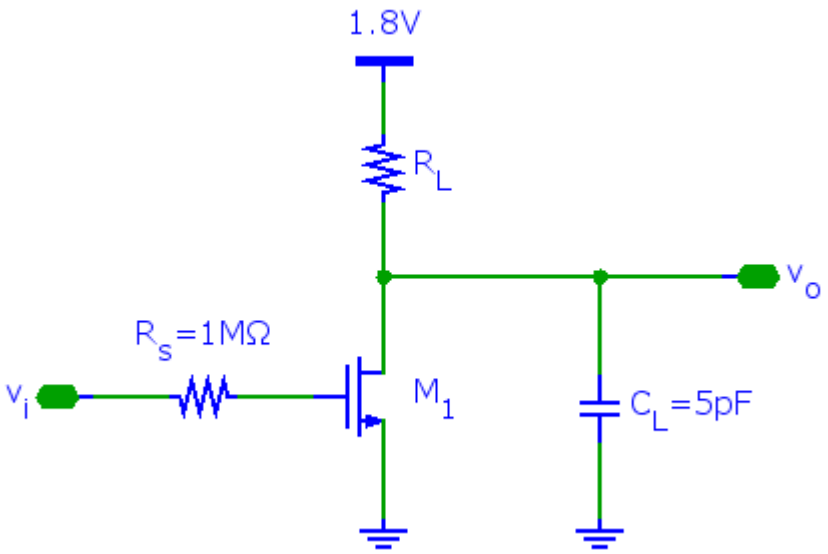
Bernhard E. Boser
boser@eecs.berkeley.edu

Overview

- Traditional analog design methodologies typically require iteration
  - "Square Law" design equations are inaccurate for submicron devices
  - Depend on poorly defined parameters: μC_{ox}, V_{th}, V_{dsat}, …
  - Difficult to achieve an "optimum" (e.g. minimum power)

- g_m/I_d-based design
  - Links design variables (g_m, f_t, I_d, …) to specification (bandwidth, power)
  - Employs design charts to accurately size transistors

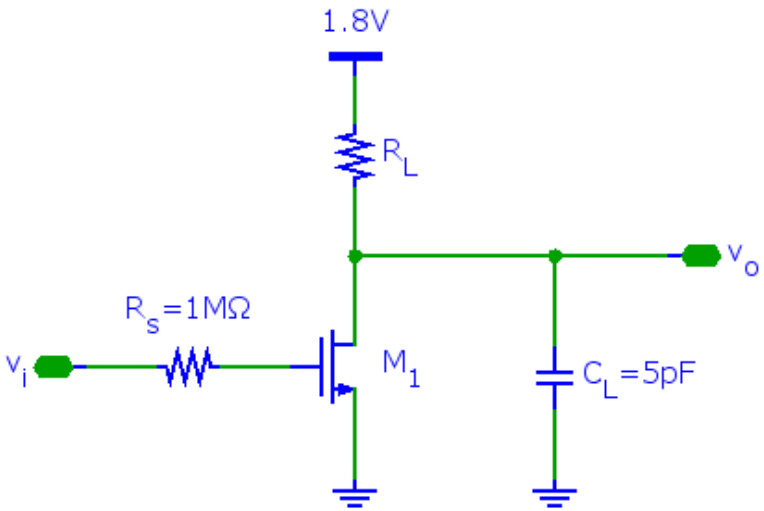
Motivation: A design example



Specifications:

- Small signal gain: $a_v = v_o/v_i = 5$
- Bandwidth: $B \geq 10\text{MHz}$
- Source resistance: $R_s = 1\text{M}\Omega$
- Load capacitance: $C_L = 5\text{pF}$
- Minimum power dissipation

Design Approaches



Design equations (Square-Law model)

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2$$

$$g_m = \mu C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)$$

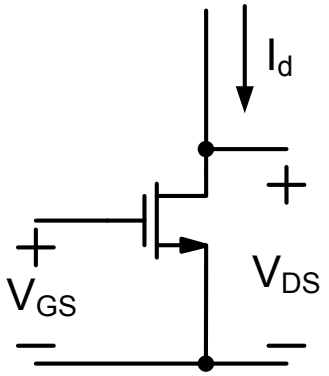
$$C_{GS} = C_{ox}WL$$

etc. ...

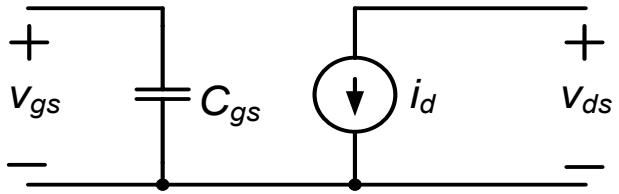
Difficulties

- Sub-micron transistors are not well described by these equations
- Non-obvious relation of model parameters to design specification
- Leads to many iterations
- What is the minimum power, anyway?

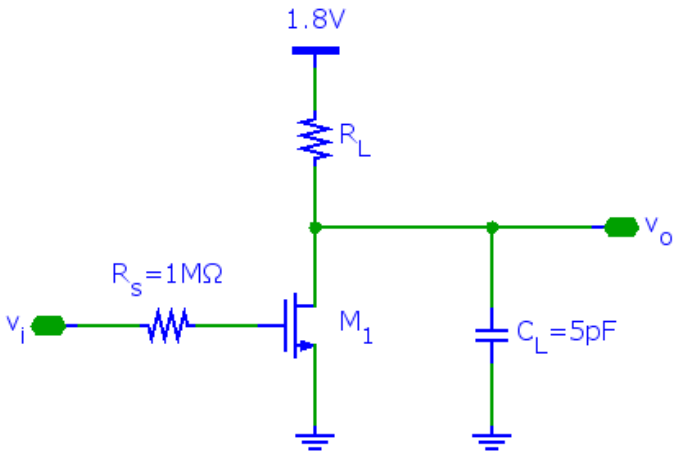
Natural Variables for Analog Design



- Transconductance g_m
- Current I_d
- Efficiency g_m/I_d
- Capacitance C_{gs}, …
- Transit frequency $f_t = g_m/2\pi C_{gs}$



Example



Design constraints

- Low frequency gain $a_v = g_m R_L$
- Pole at input $|p_{in}| = \frac{1}{R_s C_{gs}} \geq \frac{1}{2\pi B}$
- Pole at output $|p_{out}| = \frac{1}{R_L C_L} \geq \frac{1}{2\pi B}$

Specifications:

- Small signal gain: $a_v = v_o/v_i = 5$
- Bandwidth: $B \geq 10\text{MHz}$
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- Load capacitance: $C_L = 5\text{pF}$
- Minimum power dissipation

$$g_m \geq 2\pi B C_L$$

$$C_{GS} \leq \frac{1}{2\pi B R_s}$$

minimize I_d

Design Constraints and Objectives

Design constraints

$$g_m \geq 2\pi B C_L = 1.57 \text{ mS}$$

$$C_{GS} \leq \frac{1}{2\pi B R_s} = 16 \text{ fF}$$

minimize I_d

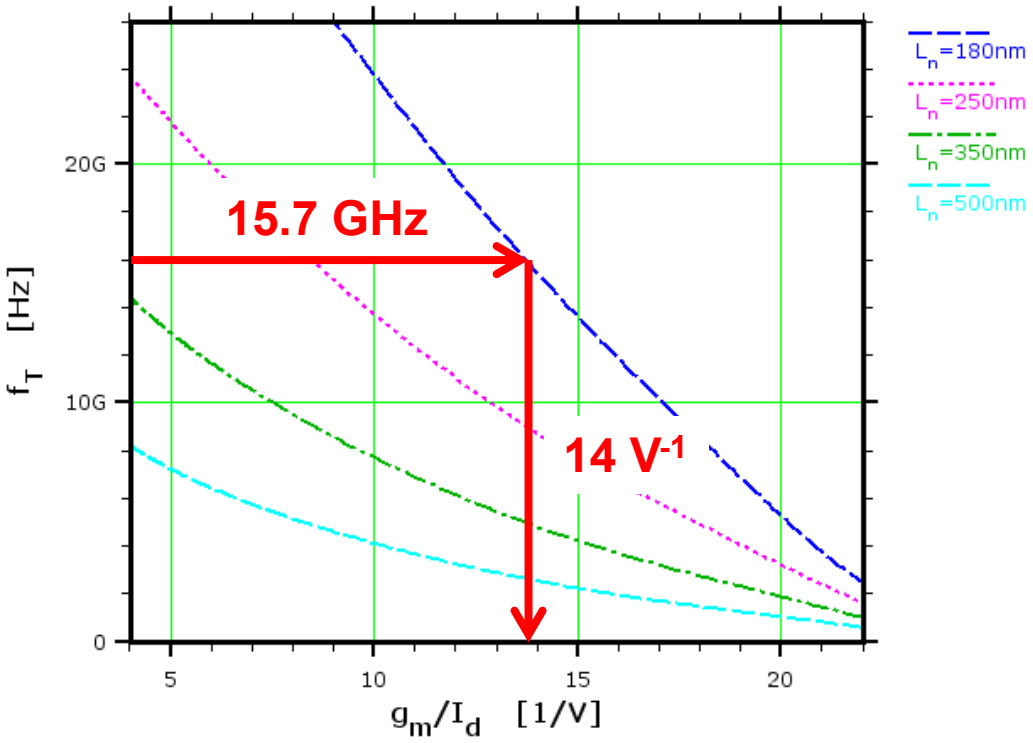
Design objectives

1. High current efficiency to minimize power $\frac{g_m}{I_d}$

2. Small C_{gs} → high f_T to meet bandwidth constraint $f_t = \frac{g_m}{2\pi C_{gs}}$

Transit Frequency f_T

f_T versus g_m/I_d tradeoff



NMOS (simulation)

Compromise

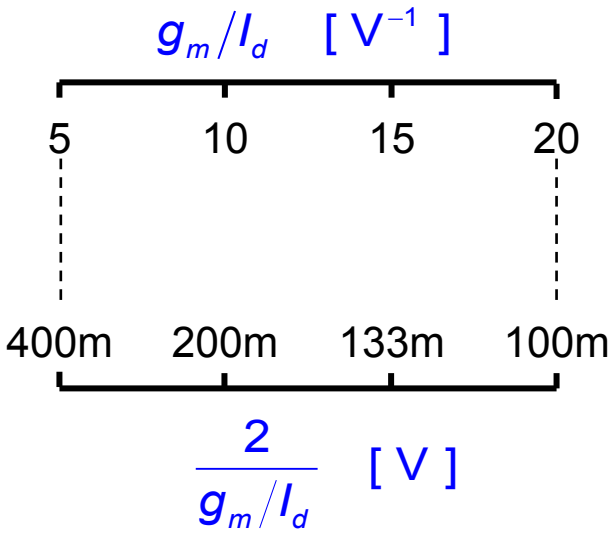
- high g_m/I_d for low power
- high f_t for low C_{gs}

Design choice

- Maximum C_{gs} to meet specification at minimum power:
  - minimum f_t
  - minimum L
  - maximum g_m/I_d

$$f_{t,\min} = \frac{g_{m,\min}}{2\pi C_{gs,\max}} = \underline{\underline{15.7\ \text{GHz}}}$$

Transistor Current Efficiency g_m / I_d



Low g_m/I_d

High g_m/I_d

- Strong Inversion
- Poor current efficiency
- Low output voltage range
- High f_t
- Small transistor

- Weak Inversion
- Good current efficiency (low V_d^{sat})
- High output voltage range
- Low f_t
- Large transistors

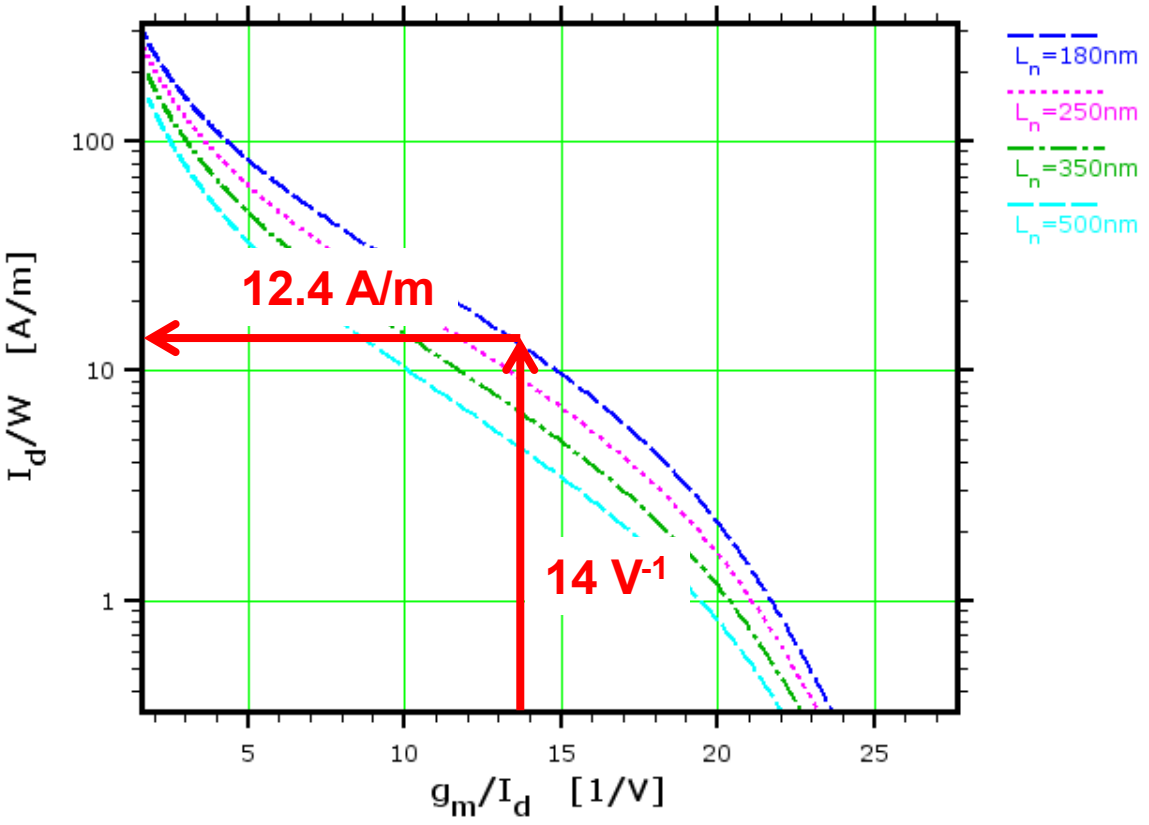
Completing the Design: Transistor Sizing

$$\frac{g_m}{I_d} = 14\ \mathrm{V}^{-1} \quad \text{and} \quad f_T = 16\ \mathrm{GHz}$$

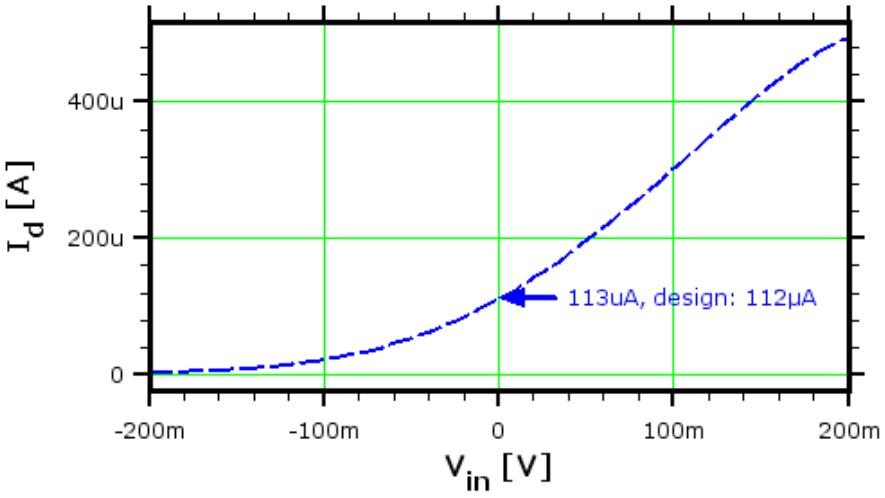
$$I_d = \frac{g_m}{g_m/I_d} = \underline{\underline{112\ \mu\mathrm{A}}}$$

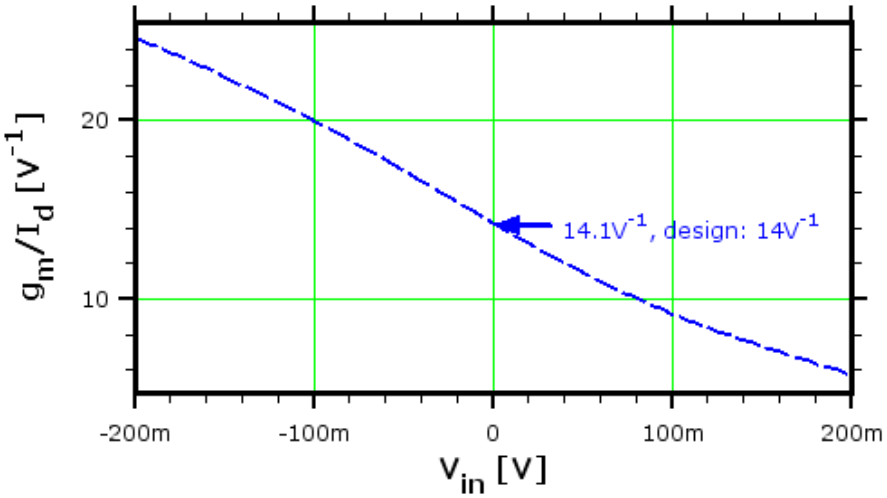
$$\frac{I_d}{W} = 12.4\ \frac{\mathrm{A}}{\mathrm{m}} \qquad \text{(from chart)}$$

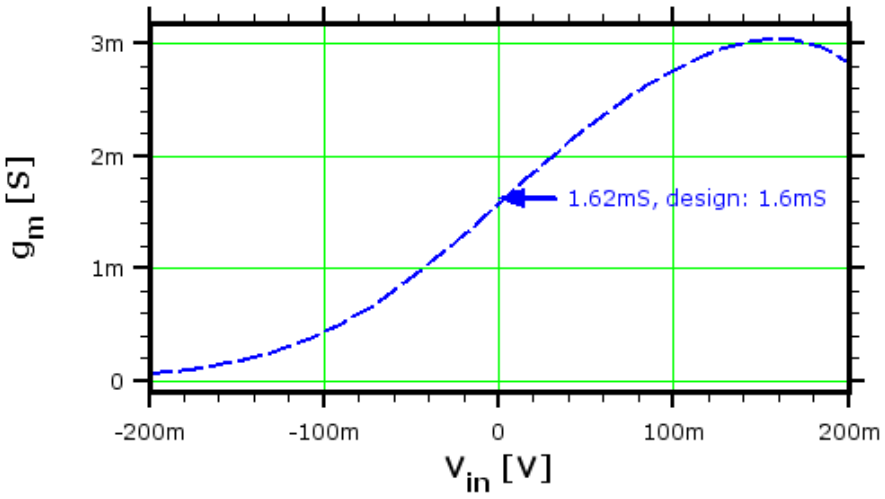
$$W = \frac{I_d}{I_d/W} = \underline{\underline{9\ \mu\mathrm{m}}}$$

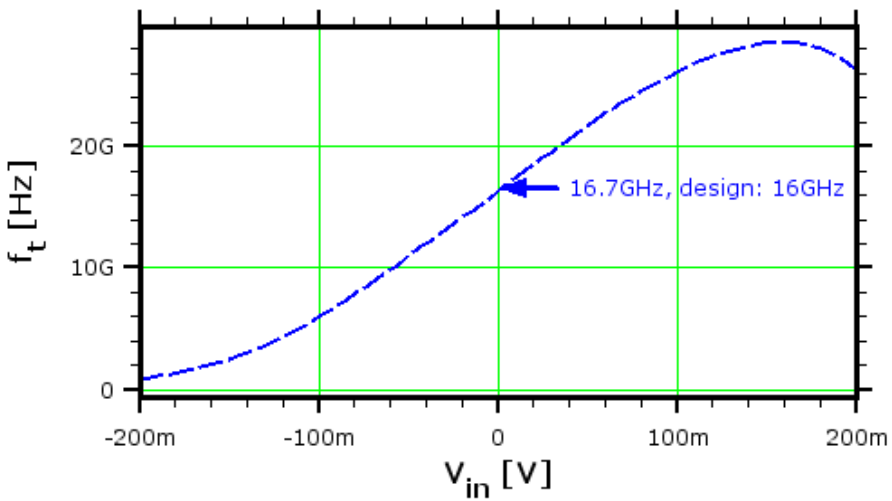


Verification: (1) Bias

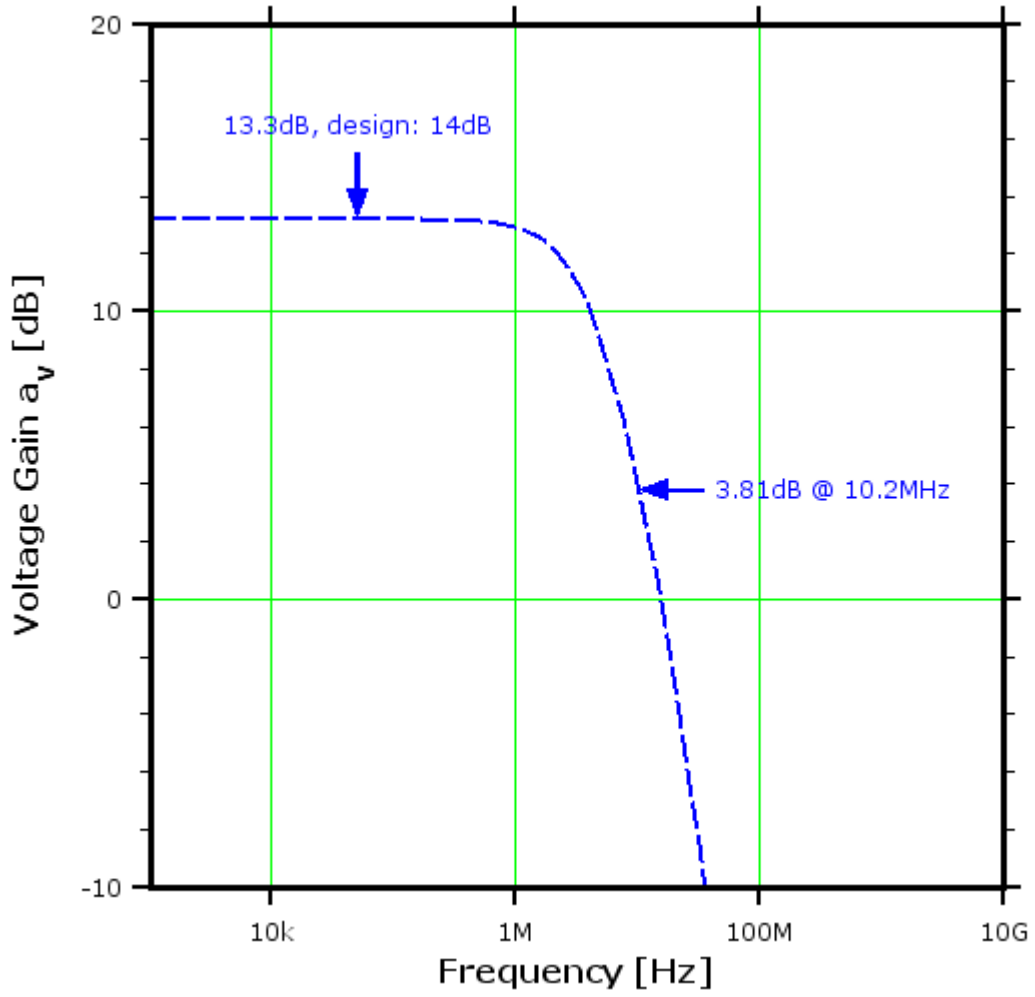








Verification: (2) Specification

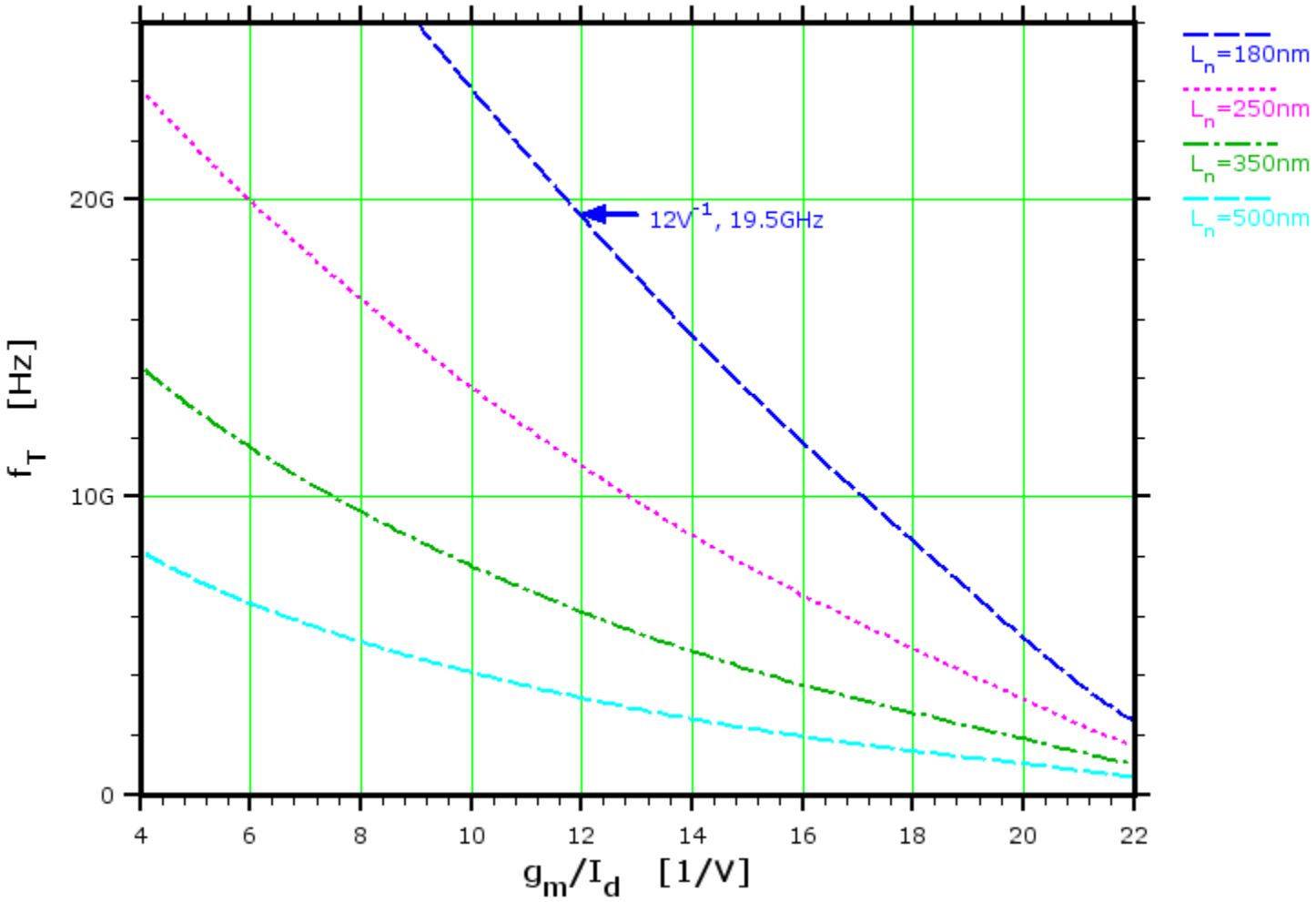


- Bias is as designed
- Gain and bandwidth slightly below spec
- Design ignored transistor r_o and self-loading
- Adjust by choosing a slightly higher f_t

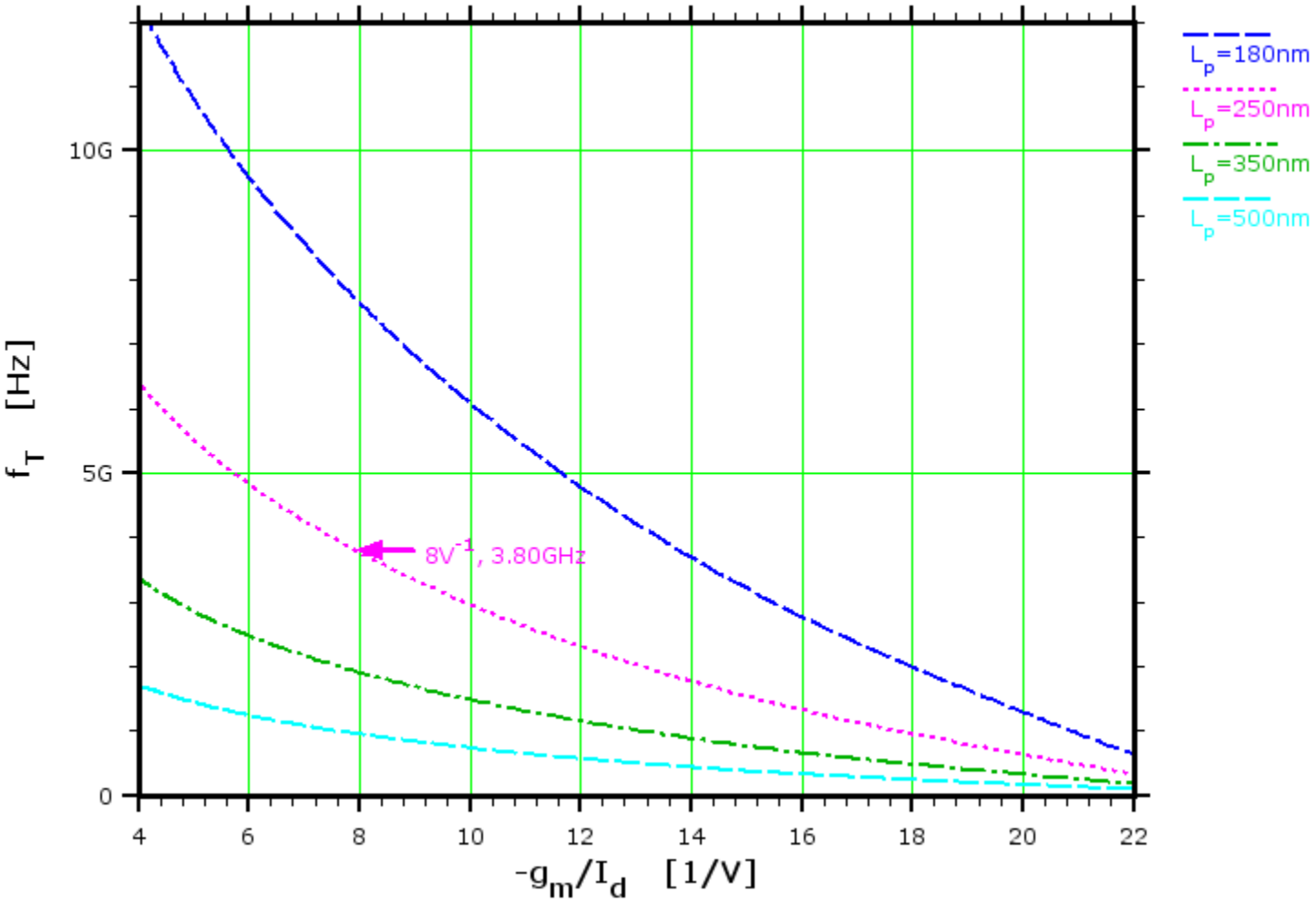
Summary

Silicon	SPICE Model	"Square Law" based design	g_m/I_d based design
Complicated Physics	Complicated Equations (BSIM, PSP, …)	Simple "Square Law" Equations	g_m/I_d & f_t Charts (process specific)
	• Accurate • Good for verification • Unsuitable for design	• Popular (textbooks) • Poor accuracy • Requires iterations • Difficult to achieve optima	• Good accuracy • Simple equations • Transistor data from charts

NMOS Transit Frequency f_T

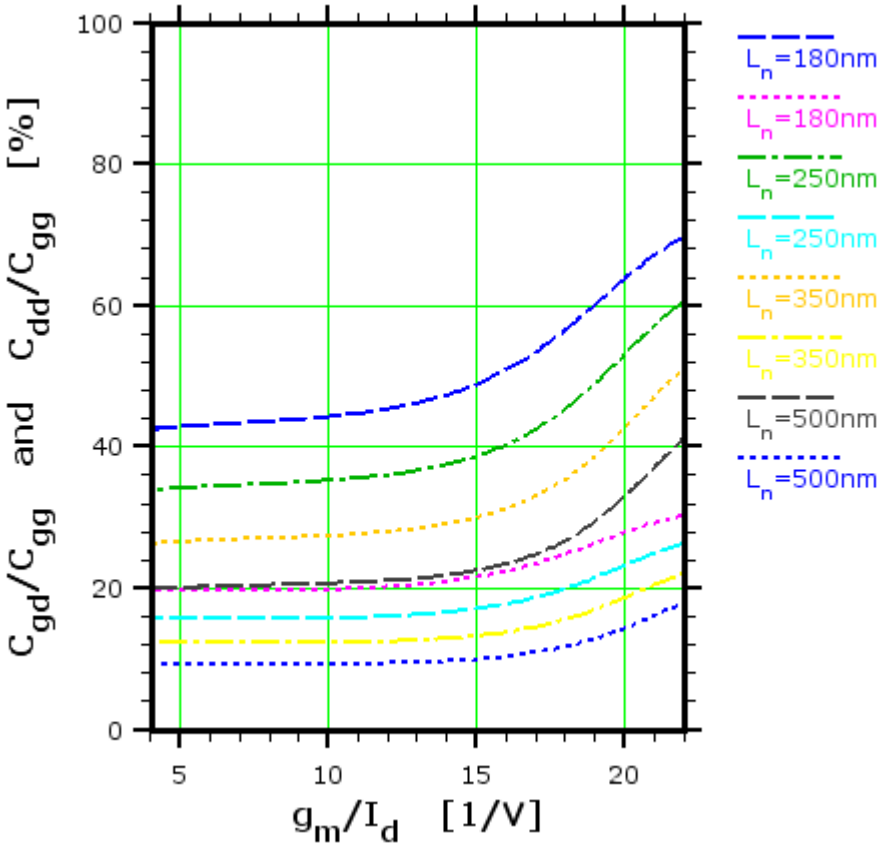


PMOS Transit Frequency f_T

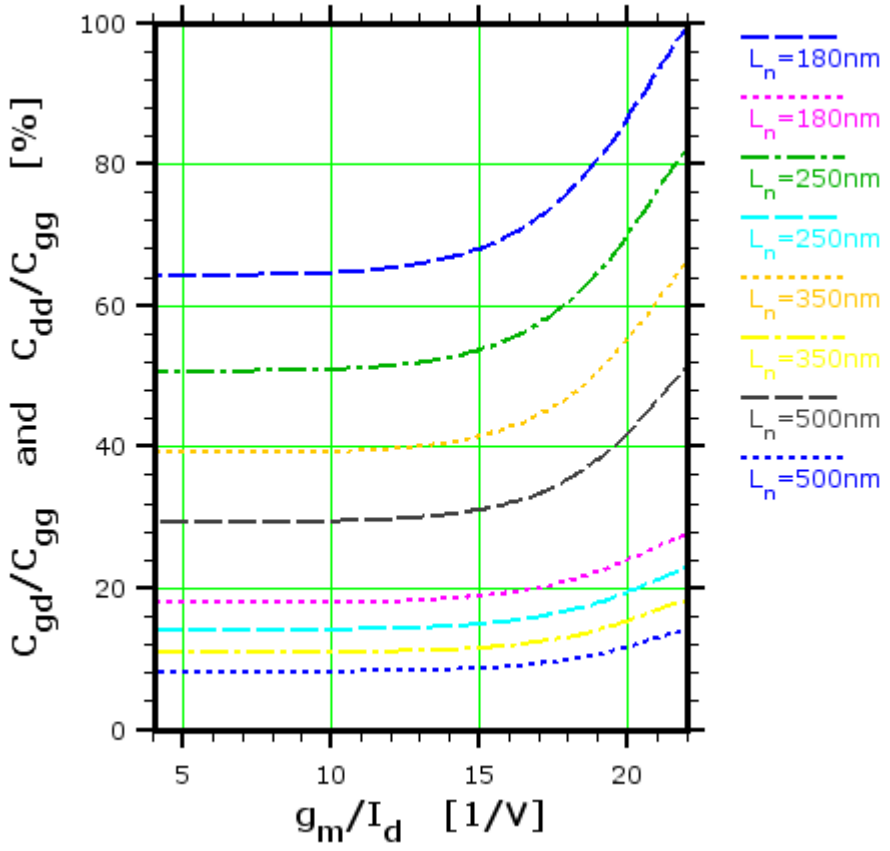


Extrinsic Capacitances C_{gd} and C_{dd}

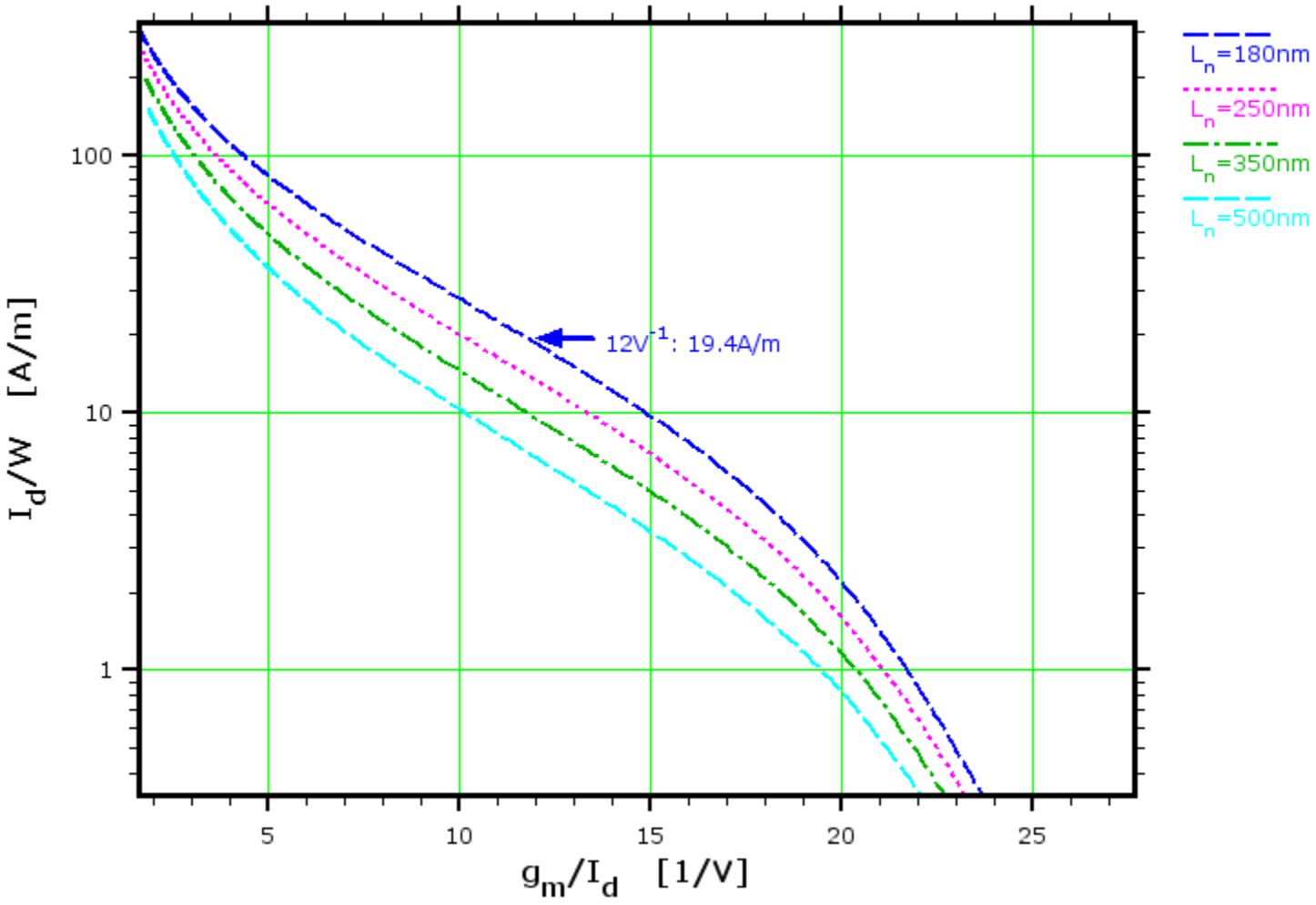
NMOS



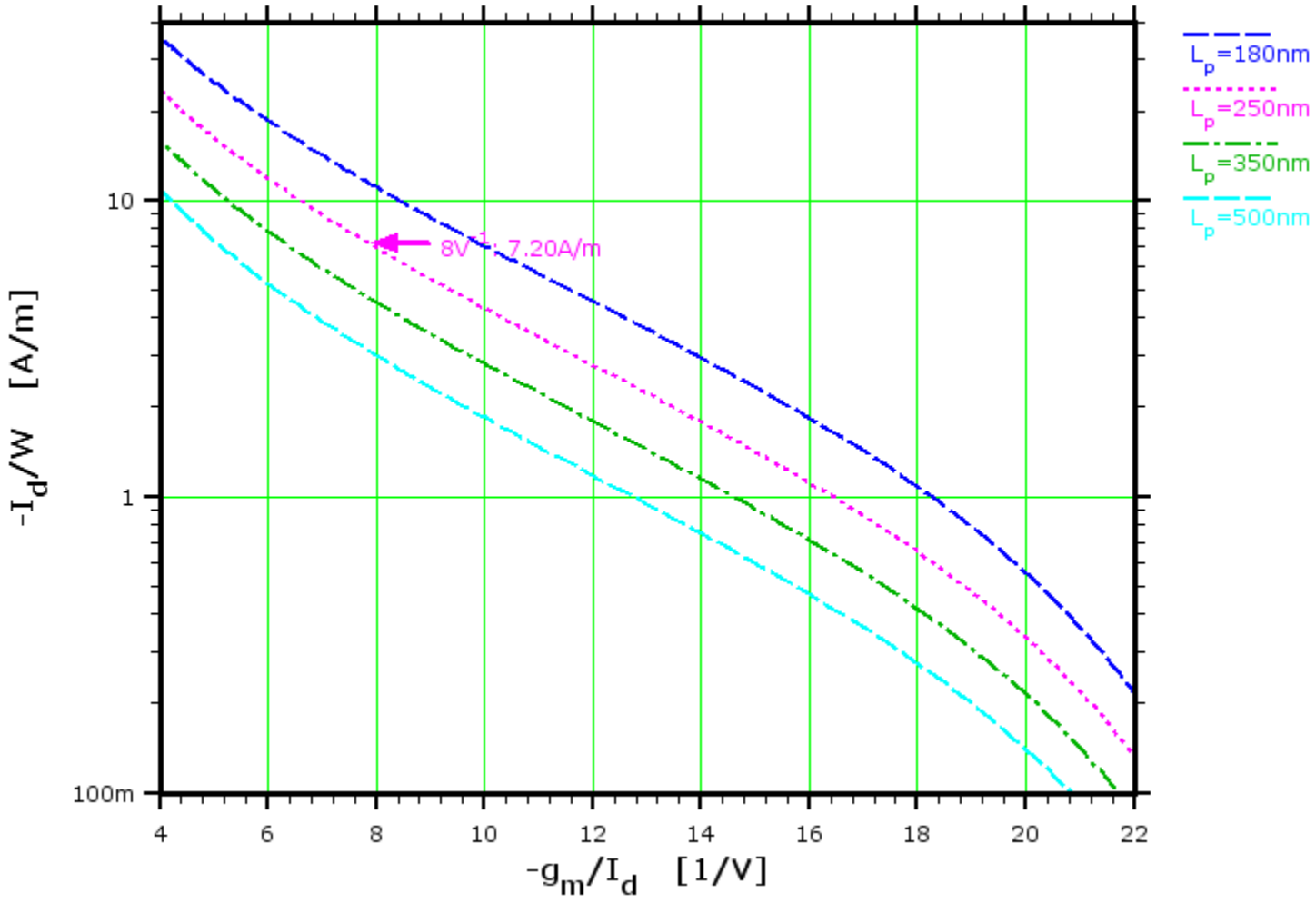
PMOS



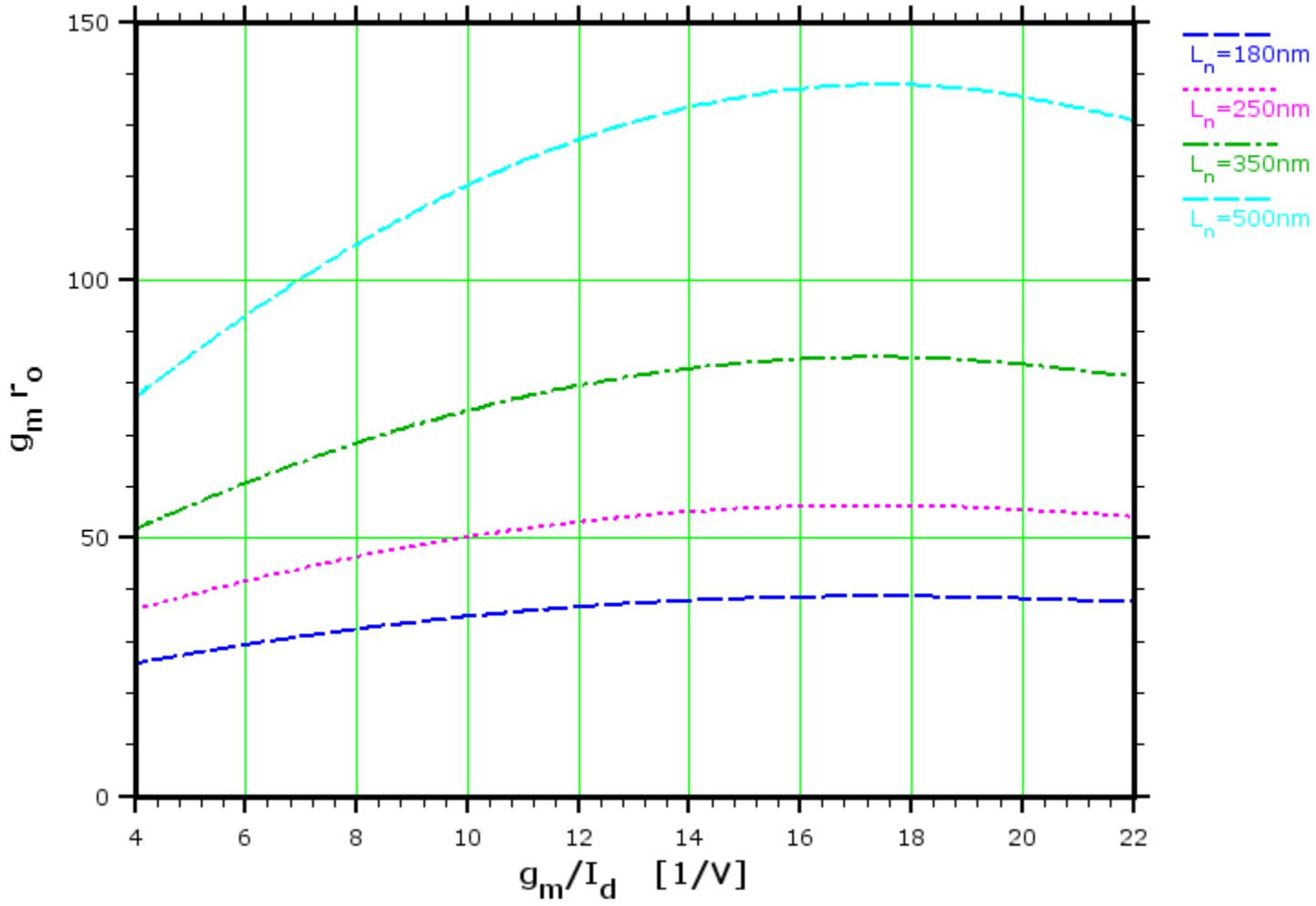
NMOS Current Density



PMOS Current Density



NMOS Intrinsic Gain $g_m r_o$



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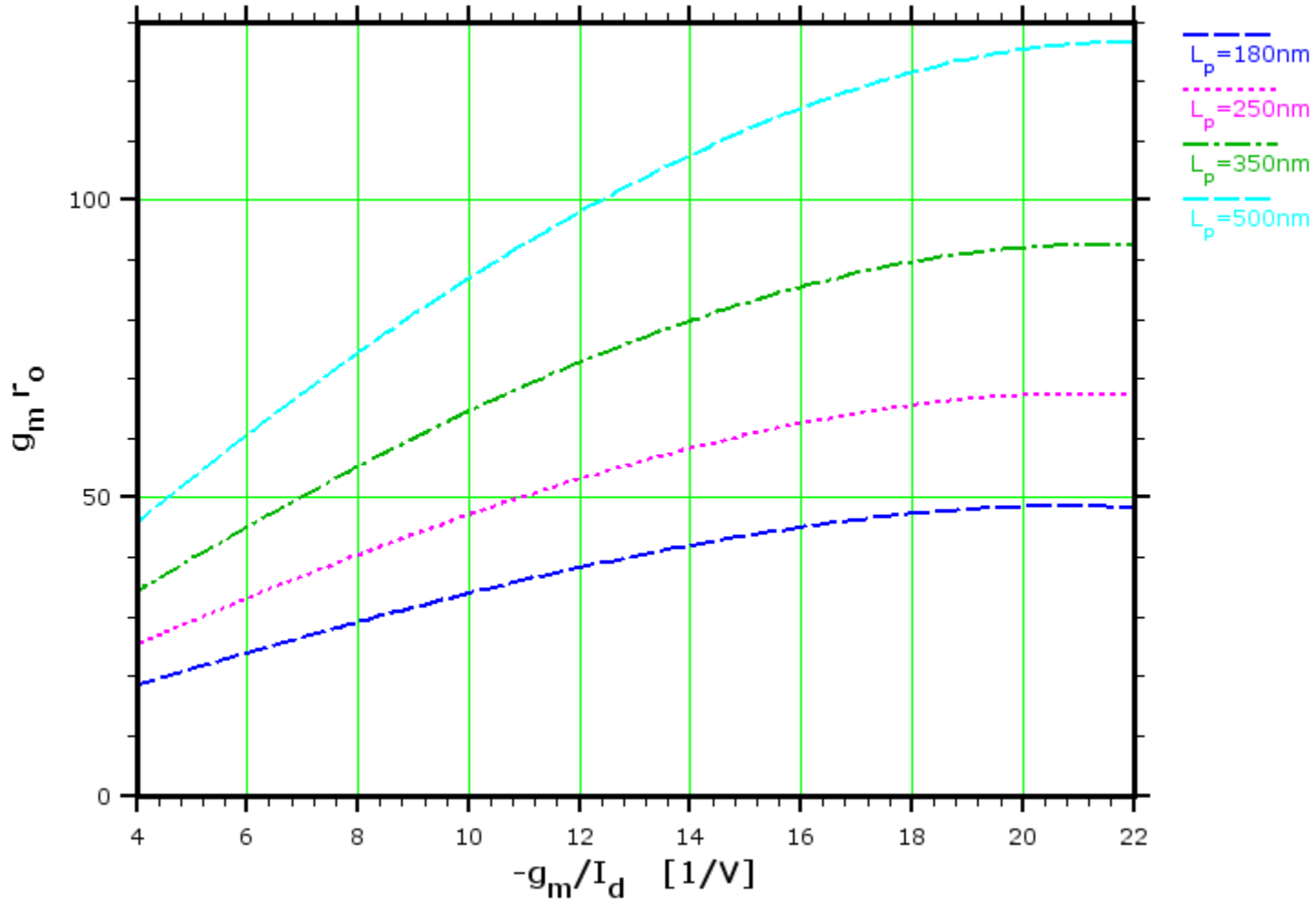

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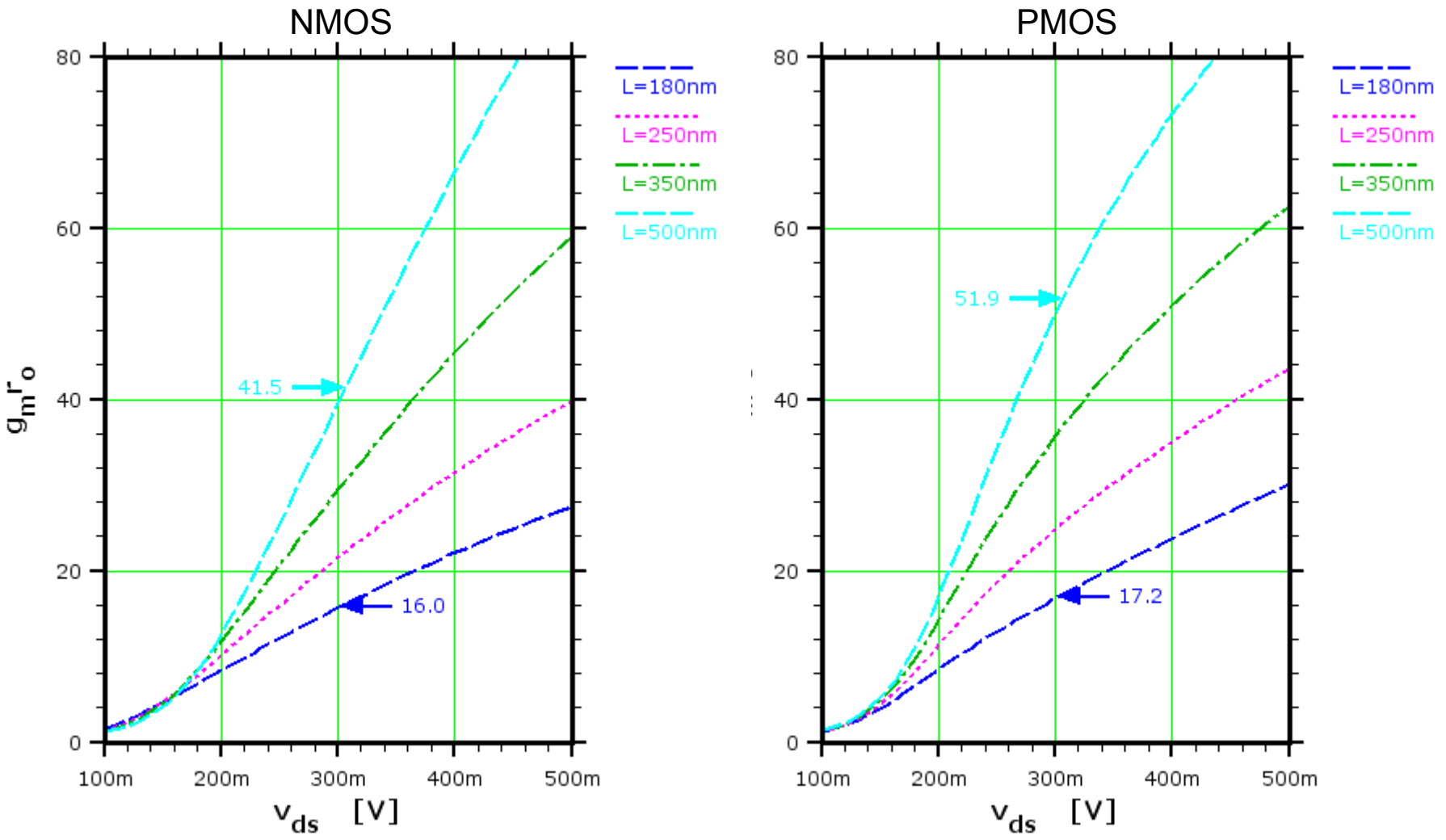
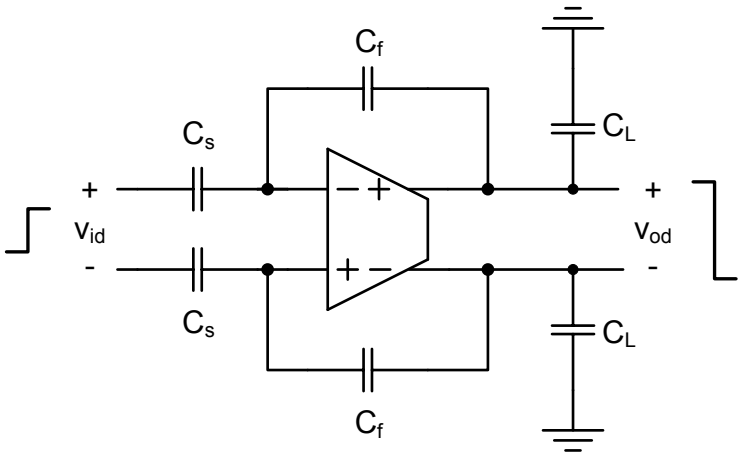


OTA Design Example

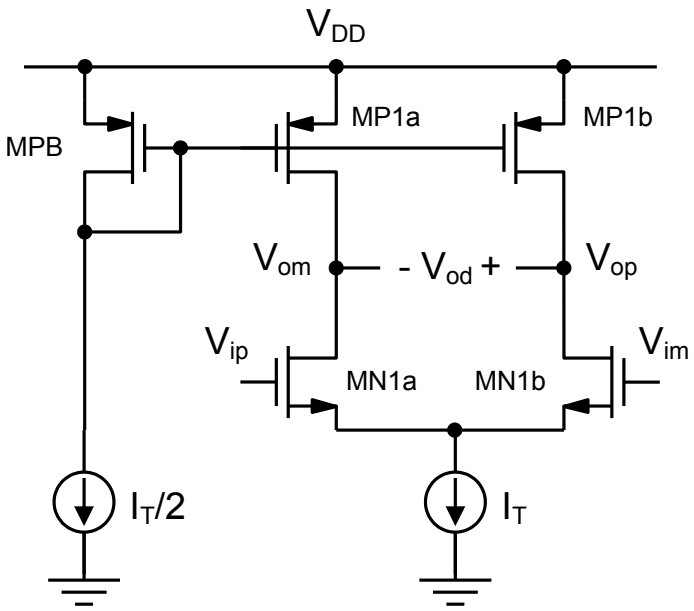


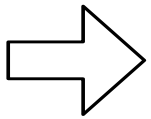
Specifications

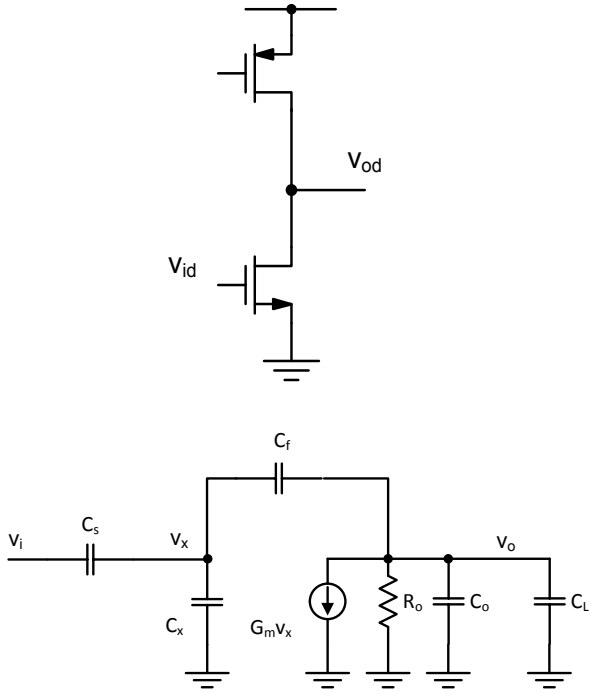
- Voltage gain $A_v = 2$
- Dynamic range $DR \geq 72\text{dB}$
- Settling accuracy $\varepsilon_d \leq 100\text{ppm}$
- Settling time $t_s \leq 10\text{ns}$

- Switched capacitor gain stage (switches not shown)
- Applications: A/D converters, filters, …

Circuit Topology







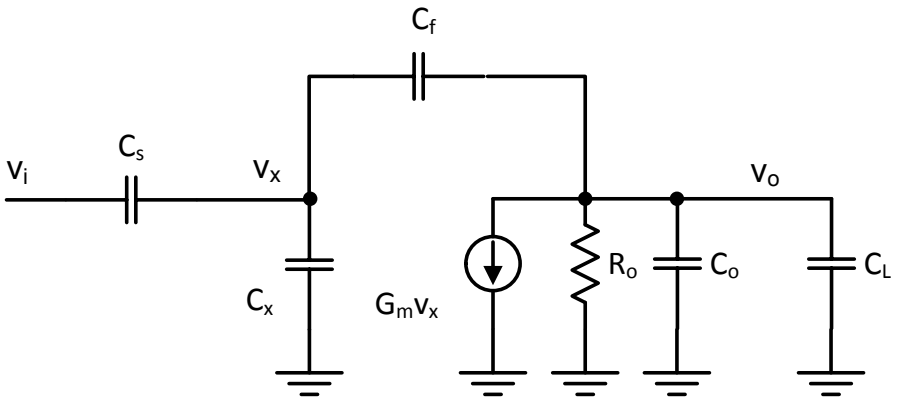
- Fully differential OTA
- Common mode and
- cascodes (for gain) not shown

- Differential mode half circuit
- Large & small signal models

Design Flow

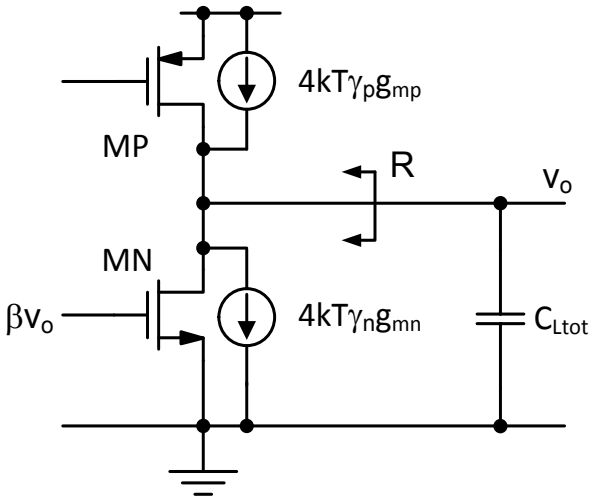
1. Determine feedback factor
2. Determine C_L to meet dynamic range requirement
3. Determine g_m to meet settling requirement
4. Pick transistor characteristics based on analysis
   - Channel length L
   - Current efficiency g_m/I_D (or f_t)
5. Determine bias currents and transistor sizes
   - I_D (from g_m and g_m/I_D)
   - W (from I_D/W, current density chart)

(1) Feedback Factor



- Open feedback loop $$\beta = \frac{v_x}{v_o} = \frac{C_f}{C_f + C_s + C_x} = \frac{1}{1 + A_v + \frac{C_x}{C_f}}$$
- C_x is amplifier input capacitance (C_{gs} + …)
  - Small C_x → large feedback factor β
  - Large C_x → low transistor f_t requirement → higher g_m/I_d → reduced current
  - Typically C_x = *(⅓ … 1) x* (C_s + C_f) (shallow optimum)

(2) Dynamic Range



Output resistance: $R \cong \frac{1}{\beta g_{mn}}$

Noise density: $\frac{\overline{v_{o,n}^2}}{\Delta f} = 4kT\gamma g_{mn}\left(1+\frac{g_{mp}/I_d}{g_{mn}/I_d}\right)\cdot\left|\frac{R}{1+j\omega RC_{Ltot}}\right|^2$

PMOS

choose $\frac{g_{mp}}{I_d} < \frac{g_{mn}}{I_d}$ for low noise

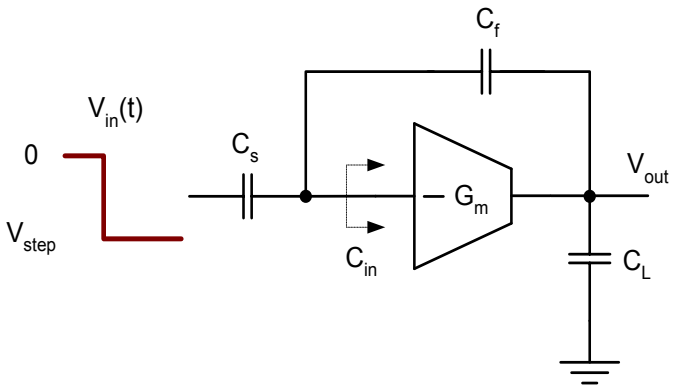
Sampled noise: $\overline{v_{o,n}^2} = \frac{1}{\beta}\frac{kT}{C_{Ltot}}\gamma\left(1+\frac{g_{mp}}{g_{mn}}\right)$

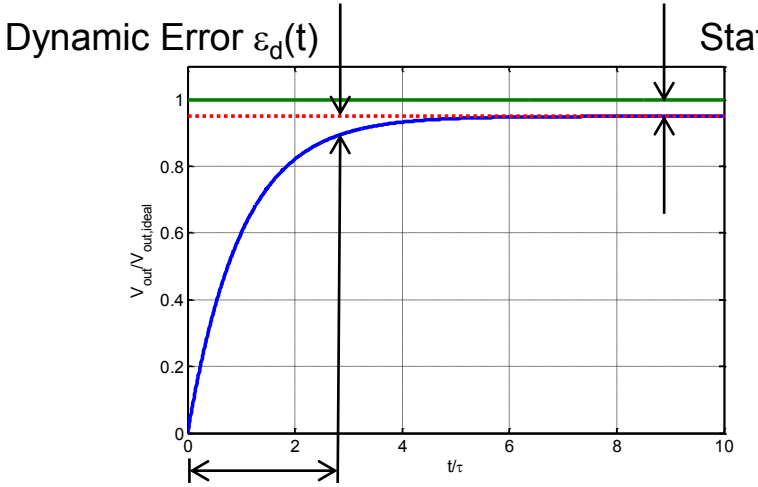
with $C_{Ltot} = C_L + (1-\beta)C_f$

Dynamic range: $DR = \frac{\frac{1}{2}V_{o,\max}^2}{\overline{v_{o,n}^2}}$

Minimum load capacitance: $C_{Ltot} \geq 2kT\frac{\gamma}{\beta}\left(1+\frac{g_{mp}}{g_{mn}}\right)\frac{DR}{V_{o,\max}^2}$

(3) Settling





$$\varepsilon_d = e^{-t_s/\tau}$$

for single pole response

Step response: $$v_{out}(t) = \underbrace{V_{step}\frac{C_s}{C_f}}_{\text{ideal response}} \cdot \underbrace{\frac{T_0}{1+T_0}}_{\text{static error}} \cdot \underbrace{\left(1-e^{-t/\tau}\right)}_{\text{dynamic error}} \quad \text{with} \quad \tau = \frac{C_{Ltot}}{\beta g_{mn}}$$

Solve for transconductance: $$g_{mn} \geq -\frac{C_{Ltot}\ln\varepsilon_d}{\beta t_s}$$

(4) Transistor Channel Length, g_m/I_d and f_t

	NMOS	PMOS	
L	180 nm	250 nm	$L_{n,min}$ reduces power
g_m/I_d	12 V^{-1}	8 V^{-1}	$g_{mp}/I_d < g_{mn}/I_d$ (noise)
f_t	19.7 GHz	3.78 GHz	$C_{gsn} < C_s + C_f$
I_d/W	18.7 A/m	7.06 A/m	

- Reduce g_m/I_d of NMOS if $C_{gsn} < C_s + C_f$
- f_t and I_d/W obtained from charts

(5) Bias Currents and Transistor Sizes

Specification

Dynamic range	$DR := 6 \cdot 12$ dB		$DR = 72$
Sampling rate	$f_s := 50MHz$	$t_s := \frac{1}{2 \cdot f_s}$	$t_s = 10\,ns$
Closed-loop gain	$A_{vo} := 2$		
Settling accuracy	$\varepsilon := 2^{-13}$	$\varepsilon = 122.07\,ppm$	$\varepsilon_d := 100ppm$
Supply voltage (min)	$V_{dd} := 1.8V$		
Sampling cap	$C_s := 200fF$	e.g. matching	$C_f := \frac{C_s}{A_{vo}}$

Transistor L, gm/Id (Guess)

Channel length	$L_n := 180nm$	$L_p := 250nm$
gm/Id	$gm\_idn := 12 \cdot V^{-1}$	$gm\_idp := 8 \cdot V^{-1}$
	$\frac{2}{gm\_idn} = 166.667\,mV$	$\frac{2}{gm\_idp} = 250\,mV$
current density (chart)	$id\_wn := 18.7 \cdot \frac{A}{m}$	$id\_wp := 7.06\frac{A}{m}$
cutoff frequency (chart)	$f_{tn} := 19.7GHz$	$f_{tp} := 3.78GHz$

Design

Feedback factor: choose $C_x := \frac{C_s + C_f}{2}$ check below!

$$\beta := \frac{1}{1 + A_{vo} + \frac{C_x}{C_f}} \qquad \beta = 0.222$$

Dynamic range: $V_{omax} := 0.6V$

$$C_{Ltot} := 2 \cdot k_B \cdot T_r \cdot \frac{1}{\beta} \cdot \left(1 + \frac{gm\_idp}{gm\_idn}\right) \cdot \frac{10^{0.1 \cdot DR}}{V_{omax}^2}$$

$C_{Ltot} = 2.644\,pF$

$$\sqrt{v_{on}^2} = \sqrt{\frac{k_B \cdot T_r}{C_{Ltot}} \cdot \frac{1}{\beta} \cdot \left(1 + \frac{gm\_idp}{gm\_idn}\right)} = 106.57\,\mu V$$

Transconductance: $g_{mn} := -\frac{C_{Ltot} \cdot \ln(\varepsilon)}{\beta \cdot t_s}$ $g_{mn} = 10.721\,mS$

$I_d := \frac{g_{mn}}{gm\_idn}$ $I_d = 893.379\,\mu A$

$C_{gsn} := \frac{g_{mn}}{2\pi \cdot f_{tn}}$ $C_{gsn} = 86.611\,fF$ < $C_x = 150\,fF$ ok!

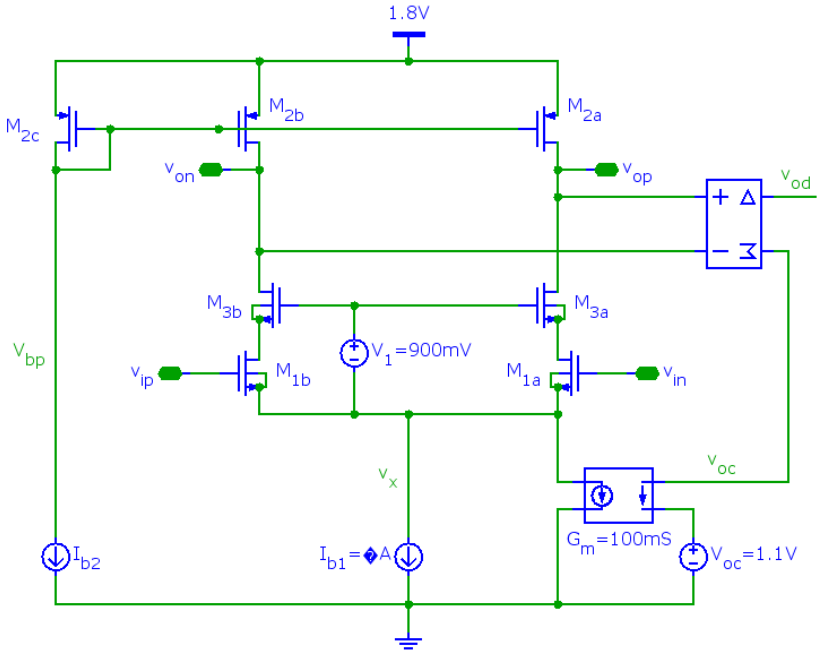
Transistor sizing ... $W_n := \frac{I_d}{id\_wn}$ $W_n = 47.774\,\mu m$

$W_p := \frac{I_d}{id\_wp}$ $W_p = 126.541\,\mu m$

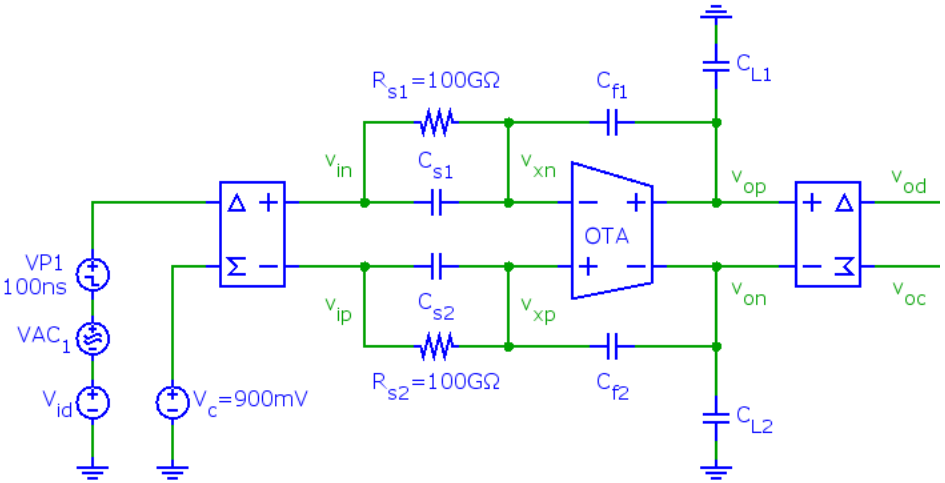
ota1.mcd

Verification: (1) Test Bed

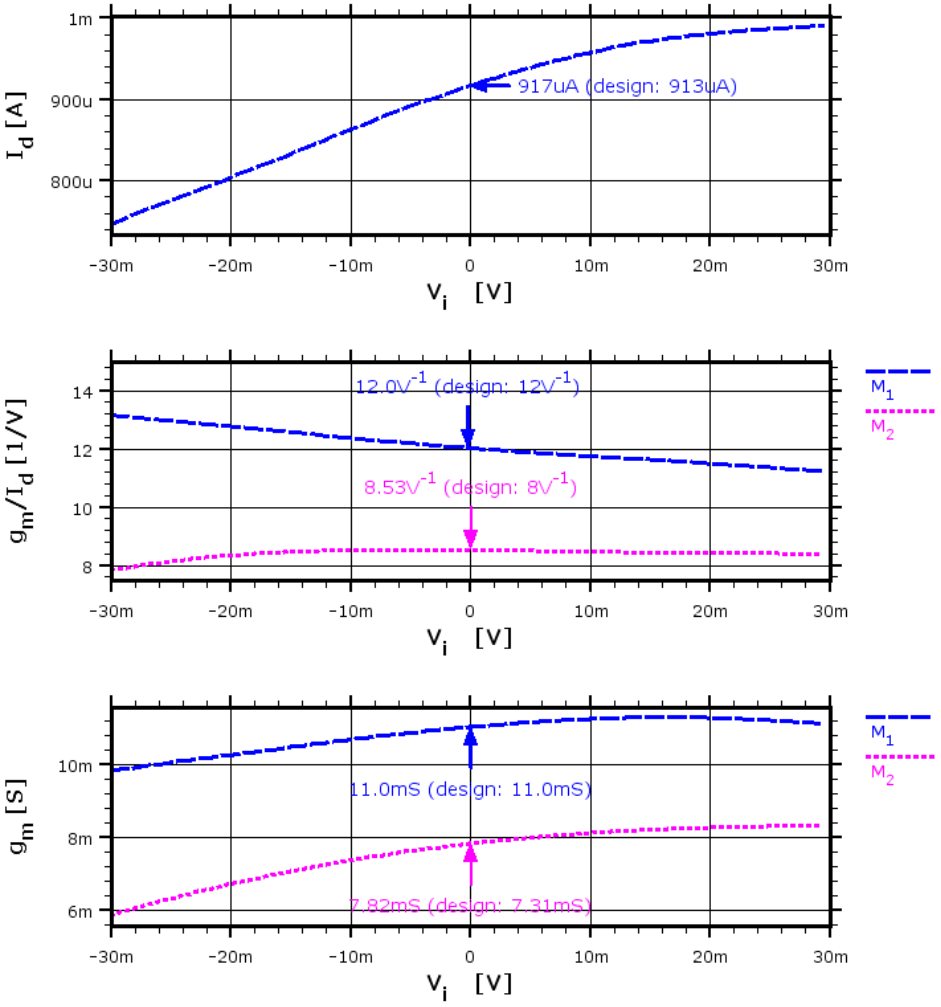
OTA



OTA in Feedback Loop

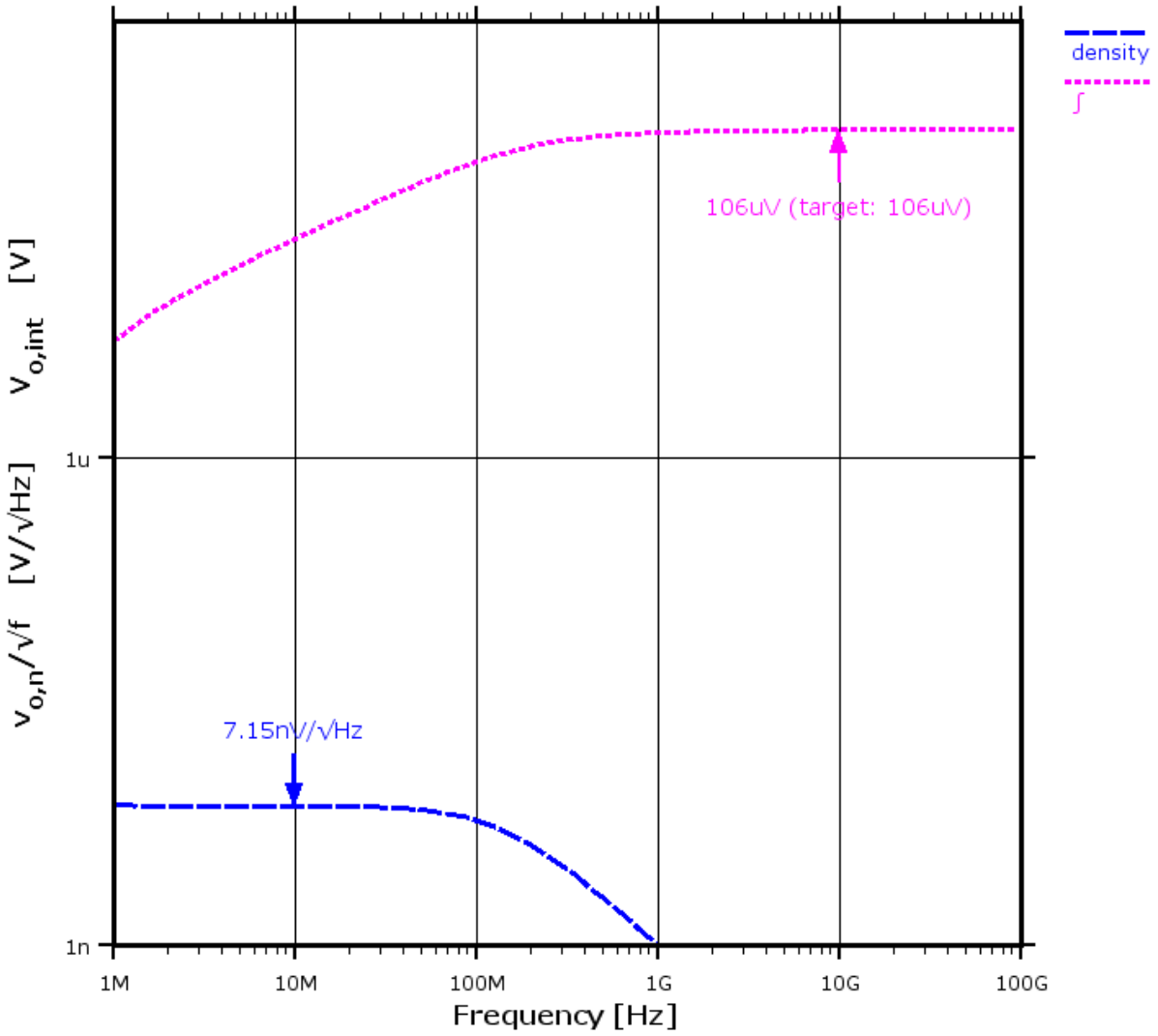


Verification: (2) Bias



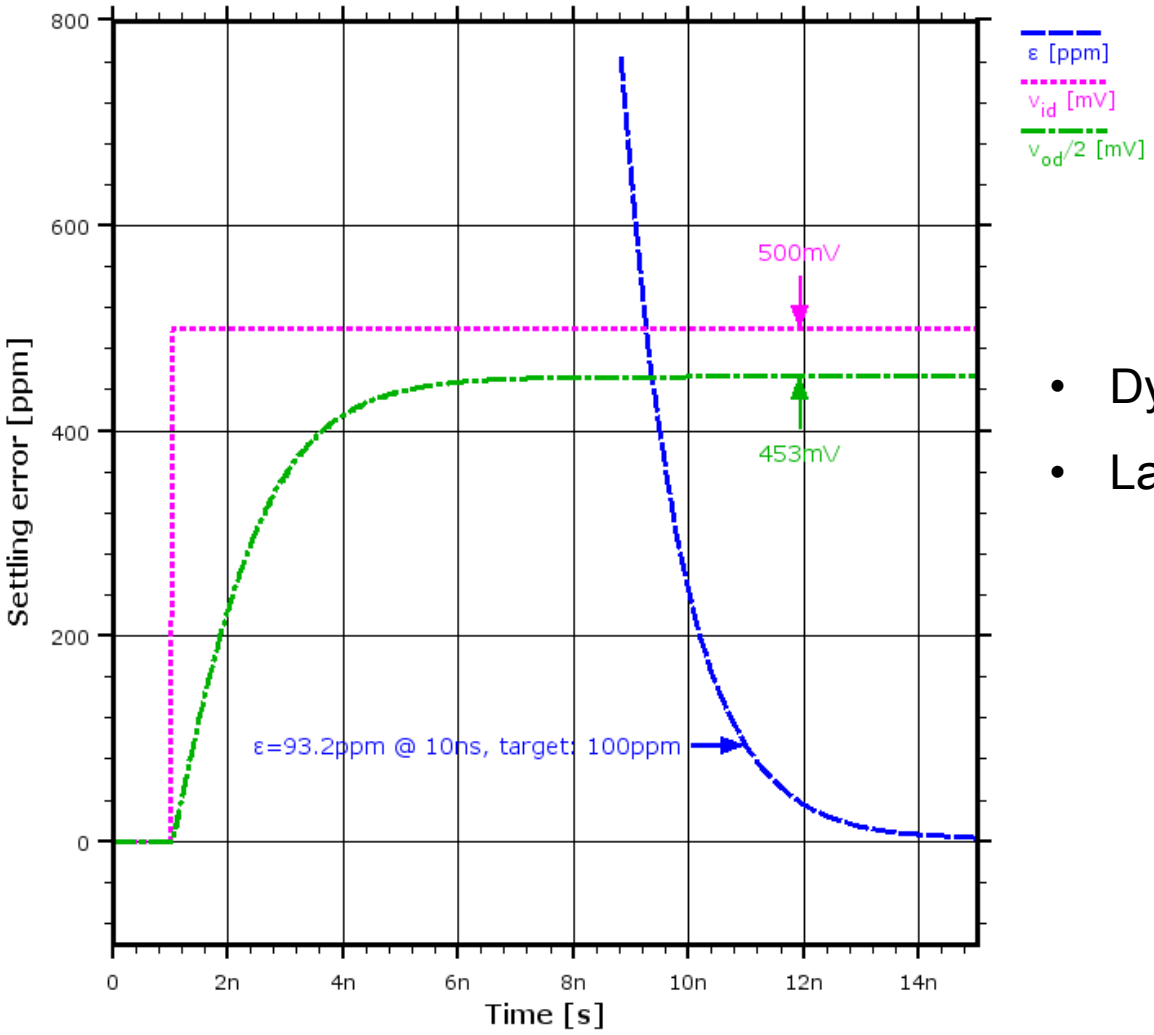
So far, so good …

Verification: (3) Dynamic Range



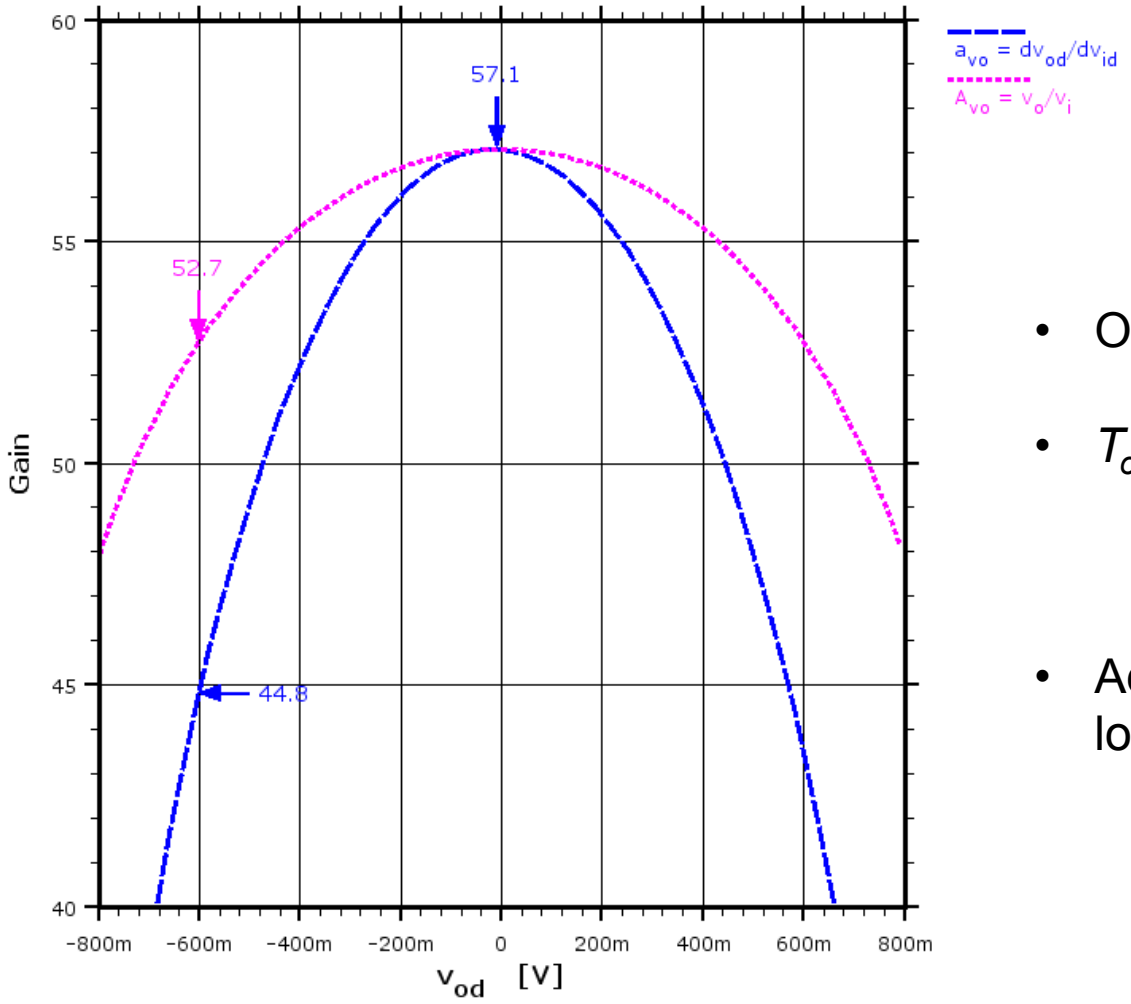
perfect!

Verification: (4) Settling Time



- Dynamic settling error target met
- Large static error ~10%

Openloop Gain



- Openloop gain only A_{vo} ~ 50
- $T_o = \beta A_{vo} = 11$
- Add cascodes to increase low frequency gain

Generic g_m/I_d-based Design Flow

1. Determine g_m from design objectives (dynamic range, bandwidth, …)
2. Pick L
   - Short channel → high f_t (high speed)
   - Long channel → high intrinsic gain, good matching, …
3. Pick g_m/I_D or f_t
   - Large g_m/I_D → low power, large signal swing
   - Small g_m/I_D → high f_t (high speed)
4. Determine I_D (from g_m and g_m/I_D)
5. Determine W (from I_D/W, current density chart)

- Adapt to design specifics

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